Attorney Docket No.: BLD920020007US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re PATENT APPLICATION of:	
Nenand Rijavec	
Appln. No.: 10/065,745	Art Unit: 2625
Filed: November 14, 2002	Examiner: Peter K. Huntsinger
For: APPARATUS, METHOD AND PROGRAM PRODUCT FOR CONTROLLING PRINTING	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop **AF**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Pursuant to an Official Gazette Notice dated, 7 February, 2006, Applicants hereby request a Pre-Appeal Brief Conference (Request) in the above identified application. This Request is being filed with a Notice of Appeal, appealing a rejection in a Final Office action (Final), dated May 18, 2007, in the above identified application. Specifically, claim 9 is finally rejected under 35 USC §101; claims 10 and 11 are finally rejected under 35 USC §112; and claims 1 – 11 are finally rejected under 35 USC §103(a) over U.S. Patent No. 6,825,943 to Barry et al. in view of U.S. Patent No. 6,315,390 to Fujii, alone, or further in combination with U.S. Patent No. 6,532,016 to Venkateswar et al. or U.S. Patent No. 5,946,460 to Hohensee et al.

Patentability of claim 9 under 35 USC §101: Claim 9 recites a "computer program **product** comprising a **computer readable medium** with program **instructions stored thereon** and effective when executed by a computer system to cause the computer system" at lines 1 – 3 (emphasis added). There is no way, of which the applicants are aware, that computer program instructions could be stored on a "carrier wave" as alleged in the Final, for example. Therefore, claim 9 is statutory[1].

[1] "[A] claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory." See *Lowry*, 32 F.3d at 1583-84, 32 USPQ2d at 1035.

Patentability of claims 10 and 11 under 35 USC §112: Specifically, the Final asserts that the specification, as filed, would not convey to a skilled artisan that the "sequencer [remains] unchanged by additions and removals of connected and disconnected said raster image processors.[2]" Prior to filing an RCE that included claims 10 and 11, enablement was not raised. Therefore, it has been established that the application, as filed, "[enables] any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, … .[3]" Applicant notes that this requirement, "to make and use the same,[4]" is not directed at the claims, but to making and using that which is claimed.

As recited by the present application, "each controller can be configured, by adding RIP machines and connecting networks, to suit the needs of each customer.[5]" Claims 1 and 5 (from which claims 10 and 11 depend) recite that the "sequencer (21) … has an output port networked and communicating with, and directly connected to, the input ports of said plurality of raster image processors (22a-n) and an input port receiving a print data stream[6], … ." The sequencer (21) output port and the raster image processor (22a-n) input ports are represented in Figure 2 by the common connection between them. While changing the number of nodes on a network changes the network, it does not change the nodes on the network. Yet the Final alleges that, "adding RIP machines and connecting networks, to suit the needs of each customer" changes the sequencer 21. If this is so, enablement requires that however the sequencer is being changed must be found in the specification as filed. Otherwise, how could the written description enable "each controller [being] configured, by adding RIP machines and connecting networks, to suit the needs of each customer." However, since it has been established that the application, as filed, is enabling under 35 USC §112, the application supports that the "sequencer [remains] unchanged by additions and removals of connected and disconnected said raster image processors." Therefore, claims 10 and 11 are enabled[7] by the application as filed.

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[2] Claims 10 and 11.
[3] 35 USC §112, first paragraph
[4] *Id.*
[5] Application as filed, page 3, lines 14 – 15.
[6] Lines 9 – 11 and 10 – 12, *and see*, Figure 2.
[7] Certainly, if claims had been added that recited that connecting and disconnecting raster image processors changed the sequencer changed the sequencer, those claims would have been rejected as not being enabled.

Furthermore, applicant has previously provided a proper demand[8] that authority be produced to estabish "adding/removing nodes to a network does change other nodes in that connections are now available to the nodes" as based on Official Notice[9]. No such authority was produced.

Patentability of claims 1 – 11 under 35 USC §103: Claim 1 recites "a sequencer which has an **output port** networked and communicating with, **and directly connected to**, the **input ports** of said plurality of raster image processors" at lines 9 – 11 (emphasis added). Neither Barry et al., nor any other reference of record, teaches this. Instead, Barry et al. teaches a "distributor block 118 is provided to distribute in multiple print job files, … segmented or partitioned by instruction operator 114 for processing according to separate processes in a plurality of parallel sections of the print system … .[10]" Moreover Barry et al. specifically recites that the distributor "has **several other outputs** including an output … coupled along path 146 from distributor 118 to a second RIP engine 152 … [and] an **nth** select portion 148 is also coupled from distributor 118 … to an **nth** RIP engine 154 representing the last partitioned print job file … separately processed in a parallel path.[11]" The output of the Barry et al. instruction operator 114 (which the Final alleges corresponds to the sequencer) is connected to distributor 118. It is not "directly connected to, the input ports of said plurality of raster image processors" as claim 1 recites. Further, Barry et al. specifically includes separate paths 142, 146 and 151 from the distributor 118 to the RIP engines 142. Very clearly, the Barry et al. distributor 118 is more than a "transmission line" as the Final asserts.

Further with regard to claim 1, Fujii et al. is relied upon solely to "disclose a plurality of print head drivers, … (col. 6, lines 60-65)." However, adding Fujii et al. print head drivers to Barry et al. does not change the fact the neither reference shows recites "a sequencer which has an **output port** networked and communicating with, **and directly connected to**, the **input ports** of said plurality of raster image processors[12]" as claim 1 recites. Therefore, the combination of Barry et al. with Fujii et al. fails to result in the present invention as recited in claim 1. Accordingly, *prima facie* obviousness has not been established for claim 1 under 35

[8] *Chevenard,* 139 F.2d at 713, 60 USPQ at 241 ("[I]n the absence of any demand by appellant for the examiner to produce authority for his statement, we will not consider this contention.").
[9] *See*, MPEP §2144.03.
[10] Barry et al., col. 5, lines 8 – 13.
[11] *Id*, lines 31 – 38 (emphasis added).
[12] *Supra*.

U.S.C. §103(a) over the combination of Barry et al. with Fujii et al. Since claim 3 depends from claim 1, *prima facie* obviousness has not been established under 35 U.S.C. §103(a) for claim 3 over the combination of Barry et al. with Fujii et al. for the reasons set forth with respect to claim 1 or, for any other claim depending from claim 1.

The Final relies on Venkateswar et al. in rejecting claim 2, specifically, to teach "a sequencer (main processor 52) being connected to raster image processors (parallel processors 54) (Fig. 2a).)" However, Venkateswar et al. FIG. 2a shows a single-chip multiprocessor[13] with the master processor on the same chip as the parallel processors. One could not add and subtract processors from such a single chip. Nor is the Venkateswar et al. main processor 52 networked with the raster image processors. Thus, Venkateswar et al. fails to add what is missing from the combination of Barry et al. with Fujii et al. Therefore, the combination of Barry et al. and Fujii et al. with Venkateswar et al. fails to result in the present invention as recited in claim 2, and so, *prima facie* obviousness has not been established under 35 U.S.C. §103(a) for claim 2.

Hohensee et al. is relied upon to teach that the raster image processors convert data from one form to another. So, Hohensee et al. fails to add what is missing from the combination of Barry et al. with Fujii et al. to result in claim 4, and so, *prima facie* obviousness has not been established has not been established under 35 U.S.C. §103(a) for claim 4.

None of the references of reference shows "a pipeline of elements connected between a print server and a printer and processing print control data from said print server," wherein the pipeline includes "a sequencer which has an output port networked and communicating with the input ports of said plurality of raster image processors and an input port receiving a print data stream," as Claim 5 recites. Barry et al. Fig 10, upon which the Final relies to show this, shows a printer labeled 1018 and net interface labeled 1026, and teaches that someone can print from PC 1008 to local printer 1018 connected to the PC 1008[14]. There is nothing in Barry et al or any other reference of record that has anything to do with "a pipeline of elements," much less multiple print head drivers between a print server and a printer. Fujii

[13] "One embodiment of a sort-first implementation using a **single-chip multiprocessor** is shown in FIG. 2a." col. 5, lines 45 – 46 (emphasis added).

[14] Applicants previously noted that the Barry et al. specification includes typographical errors with regard to these pictured elements.

et al., for example, shows print head drivers in a printer[15] driving print heads. Neither, does Barry et al, show or suggest "a pipeline of elements connected between a print server and a printer and processing print control data from said print server," as claim 5 further recites. Nor is this shortcoming of the combination of Barry et al. with the Fujii et al. cured by the addition of Hohensee et al. Therefore, *prima facie* obviousness has not been established under 35 U.S.C. §103(a) for claim 5 or, claim 11 or any other claim depending from claim 5.

No reference of record teaches or suggests "communicating queued packaged print stream data portions directly over a network to a plurality of raster image processors" as claim 6 recites. As noted hereinabove, Barry et al. teaches communicating through a distributor, not "directly over a network;" Fujii et al. is not concerned with communications to the raster image processors; and, Venkateswar et al. teaches on-chip communications[16]. Therefore, *prima facie* obviousness under 35 U.S.C. §103(a) has not been established for claim 6 or, claims 7 – 9 depending therefrom.

Independent review and consideration is respectfully solicited. Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-3669 and advise us accordingly.

Respectfully Submitted,

August 20, 2007
(Date)

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[15] See, e.g., Venkateswar et al. col. 3, lines 31 – 32 ("FIG. 3 is a block diagram of an embodiment of a control circuit **in** a printer." Emphasis added).
[16] As previously noted, the arrow from scheduling in the Venkateswar et al. master processor to Boundary Processing Rasterization in the Venkateswar et al. parallel processors is not a network within the plain meaning in the art.